Self-integration of nanowires into circuits via guided growth

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The ability to assemble discrete nanowires (NWs) with nanoscale precision on a substrate is the key to their integration into circuits and other functional systems. We demonstrate a bottom-up approach for massively parallel deterministic assembly of discrete NWs based on surface-guided horizontal growth from nanopatterned catalyst. The guided growth and the catalyst nanopattern define the direction and length, and the position of each NW, respectively, both with unprecedented precision and yield, without the need for postgrowth assembly. We used these highly ordered NW arrays for the parallel production of hundreds of independently addressable single-NW transistors, showing up to 85% yield of working devices. Furthermore, we applied this approach for the integration of 14 discrete NWs into an electronic circuit operating as a three-bit address decoder. These results demonstrate the feasibility of massively parallel “self-integration” of NWs into electronic circuits and functional systems based on guided growth.

T
he sustained progress in semiconductor technology introduces new challenges associated with the scaling and functionality of nanosize components. In the face of these challenges, alternative unconventional device and fabrication concepts based on bottom–up assembly of synthetic nanostructures are being intensively explored (1). These nanostructures, such as quantum dots (2), nanotubes (3), and nanowires (NWs) (4), can be chemically synthesized with exquisite control over their structures and properties down to the atomic level. On the other hand, their self-assembly alone is unlikely to produce the arbitrary geometries and long-range order that are required for their integration into functional systems. To realize such systems, bottom-up assembly may be used as a complementary step in a sequence of top–down fabrication processes. Such a hybrid top–down/bottom–up approach can be based on the directed self-assembly of building blocks onto a lithographically produced template to fit the design of an integrated functional system. Thus, the building blocks integrate themselves into the system, as one of the layers in the overall design. Here we demonstrate the feasibility of this “self-integration” concept with the parallel fabrication of large numbers of devices and complex circuits, based on guided growth of horizontal NWs (5).

NWs are attractive building blocks for the bottom–up assembly of nanoscale devices and functional systems with potential applications in nanoelectronics (6), photonics (7), renewable energy (8), and biology (9). They can be synthesized with precisely controlled nanoscale dimensions and chemical compositions (10). Moreover, they may be structured to possess unique electronic properties, such as ballistic conductivity due to confinement of a 1D charge-carrier gas in core-shell NWs (11). The potential of NW-based electronics has been demonstrated for various NW materials (12). However, most studies were done at the single-device level. The main obstacle toward NW integration into large-scale electronic circuits has been the challenge to deterministically organize discrete NWs into ordered arrays according to a predefined system design. Up until now, most strategies for producing such arrays were based on postgrowth assembly in liquid by different methods, including (i) dielectrophoretic deposition between microfabricated electrodes (13), (ii) mechanical shearing onto patterned chemical functionalities (14, 15), and (iii) liquid flow inside microfluidic channels (16). The first approach (i) enables high-yield and precise positioning, but the patterned electrodes required for dielectrophoresis are an obstacle for subsequent integration of the assembled NWs into circuits. The other two approaches (ii and iii) enable highly controlled NW orientation (15) but only partial control of the NW position, where the ends of each NW are not precisely positioned in both x and y coordinates. Therefore, integration of these NWs in multidevice circuits usually requires their mapping by high-resolution microscopy, tailored design of electrodes to fit the scattered positions of each and every NW in the system, and electrode nanofabrication by electron-beam lithography (17). The need for this serial process precludes the large-scale integration of discrete NWs into functional multidevice systems.

In this work, we demonstrate a conceptually unique bottom-up approach, by which NWs are deterministically assembled during their growth, with no need of any postgrowth assembly or manipulation. The approach is based on a previously proposed concept of “vectorial growth” (18), whereby the formation of a 1D nanostructure on a substrate is defined in the form of a vector—that is, having an origin (x, y), a direction (φ), and a length (L) (Fig. L4). Although this concept was initially aimed at producing ordered arrays of carbon nanotubes (18), its practical implementation was frustrated by the low yield of nanotube nucleation, which eventually prevented the integration of functional systems based on such arrays (19). Here, we have successfully applied the vectorial growth concept to produce large ordered arrays of perfectly placed discrete NWs, thanks to the high yield of NW growth from patterned catalyst nanoparticles. We used these arrays for the parallel fabrication of a large number of NW-based devices, as well as for their integration into complex logic circuits.

Implementation of the vectorial growth concept requires independent control of each of the vector parameters, (x, y), φ, and L. Recently, we reported the guided growth of perfectly aligned horizontal GaN and ZnO NWs on different planes of sapphire (5, 20). The growth directions and crystallographic orientations of the NWs were determined by their epitaxial relationship with the substrate, as well as by a graphoepitaxial effect that guided their growth along surface steps and grooves. Owing to the single-crystal nature of the substrate, the guided growth enables control over the NW direction (φ) with extremely high accuracy and long-range order.
To reach the second milestone toward the ability to perfectly control the location of the NWs, in this work we define their origins \((x, y)\) by nanolithographically patterned catalyst nanoparticles. “Seed” catalyst dots of appropriate size and shape can be used to grow arrays of discrete NWs, with the direction defined by the guided growth and the position defined by the original location where the dots are patterned (Fig. 1B). This deterministic definition of the NW array geometry enables the realization of large-scale, multidevice, functional systems, as schematically described in Fig. 1C. The system design consists of a few sequential lithographic layers. The first layer refers to the catalytic seed nanopattern that determines the positions of each NW. The following layers refer to the device electrodes and interconnects, which are globally registered to the first layer.

**Results and Discussion**

We demonstrate the production of NW arrays with controlled position, orientation, and length by guided growth of horizontal ZnO NWs from Au nanodot arrays on R-plane sapphire substrates, that is \(α-Al_2O_3(1\bar{1}02)\) (Fig. 2A and B). Before we patterned the catalyst seeds in a fully parallel process, we performed a series of prototyping experiments to optimize their dimensions. To this end, the Au nanodots were at this stage produced by electron-beam lithography, followed by Au evaporation and liftoff (Fig. S1). Vapor–liquid–solid (VLS) growth from the Au nanodots (Materials and Methods) led to the formation of discrete, parallel ZnO NWs directed along opposite \(±[1\bar{1}01]\) crystalline directions of the R-plane sapphire (20) (Fig. 2A and B). This controlled growth also leads to highly uniform NW length \((L)\), so that both ends of each NW are precisely positioned in both \(x\) and \(y\) coordinates. Different seed dot sizes and shapes, as well as the evaporated Au thicknesses, were examined to optimize the NW yield for arrays with different periods down to 2 μm, as shown in Fig. 2A (see SI Results and Discussion for additional discussion). Ideally, two oppositely directed NWs grow from each seed dot. A yield of 96% was achieved for an array of Au rectangles of 430 nm \(×\) 140 nm size, with the long side along the NW growth direction. We found that the yield can be further increased using wider catalyst features, while paying the penalty of having double or multiple NWs grown from each dot. We speculate that Ostwald ripening during the dewetting of the catalyst thin film (21) may play a role in limiting the minimum dimensions and spacing of the catalyst nanodots that are required for high-yield growth of discrete NWs.

To quantitatively characterize the NW positioning accuracy, we separately estimated the uniformity of the three vector parameters for more than 100 NWs in an array (Fig. S2). First, we found that the NW length is distributed with a SD of 11.7% around its average value of \(\sim 6\) μm. This length uniformity is substantially higher than previously reported for GaN and ZnO NWs grown from continuous catalyst films (5, 20). We may speculate about several possible reasons for this improvement. First, the dewetting time of the nanopatterned catalyst was 1 min (Materials and Methods) versus 5 min for the continuous catalyst film. Because the Ostwald ripening is a time-dependent process (22), shorter dewetting is expected to produce more uniform nanoparticles, which ensures simultaneous nucleation at the solid–liquid–gas interface from all of the nanoparticles, as well as a more uniform growth rate (23). As for GaN NWs, they were aimed to be two orders of magnitude longer compared with those of ZnO, and thus had a higher probability to be stopped during the growth by random surface defects, showing significantly larger length distribution.

The accuracy in the lateral position (i.e., perpendicular to the NW axis) was characterized in terms of the NW misplacement from their positions defined by the array design (Fig. 2D). With more than half of the NWs placed within \(±50\) nm from their nominal positions, the obtained accuracy is unprecedented compared with the previously reported methods of NW assembly (17). As to the direction accuracy, more than 99% of the NWs were found to be aligned within \(±0.1°\). Previously reported methods for NW alignment, such as mechanical (24), blown bubble (25), flow
followed by angle-evaporated-mask imprinted with a cast polydimethylsiloxane (PDMS) soft mold, imprinted Au dots (Fig. S4) were used for transistor fabrication, done by photolithographic patterning of source, drain, and top-gate electrodes (Fig. 3 B–D). We obtained an overall yield of 85% (i.e., 85 working transistors out of 100) with typical n-type characteristics (Fig. 3E) and at least one order of magnitude on–off ratio, comparable to those of similar devices fabricated by electron-beam lithography (20). No hysteresis was observed by us during the electrical characterization of the transistors. The average transconductance at the source-drain voltage of –1.0 V and threshold gate voltage were found to be ~200 ± 80 nS (Fig. 3G), and ~7.0 ± 1.5 V, respectively (Fig. 3H). The dispersion of these device characteristics, as well as that of the on–off ratio (Fig. S5), could partly originate from the nonuniformity of the NW diameter (Fig. S6 and SI Results and Discussion). The calculated mobility and density of charge carriers were estimated to be 60 ± 30 cm²/Vs (Fig. S7) and 1.8 × 10¹⁹ ± 0.8 × 10¹⁹ cm−², respectively, consistent with previously reported data (20).

To demonstrate the scalability of NW self-integration, we prepared arrays of single-NW field-effect transistors (Fig. 3A) using exclusively parallel lithographic methods. Each array included 100 discrete NWs grown in two opposite directions from 50 seed dots. Previous reports had shown parallel device fabrication from horizontally grown NW arrays (26, 27), but each device comprised many NWs, whereas here, each transistor is built on a single NW. Nanoimprint lithography (28), which is capable of high-throughput replication of arbitrary nanopatterns with nanometer resolution, was chosen for patterning the catalyst nanodot arrays. Briefly, sapphire substrates were UV-nano-imprinted with a cast polydimethylsiloxane (PDMS) soft mold, followed by angle-evaporated-mask–assisted pattern transfer to obtain arrays of Au nanodots (29) (see Materials and Methods and Fig. S3 for details). The NWs grown from these nano-imprinted Au dots (Fig. S4) were used for transistor fabrication, done by photolithographic patterning of source, drain, and top-gate electrodes (Fig. 3 B–D). We obtained an overall yield of 85% (i.e., 85 working transistors out of 100) with typical n-type characteristics (Fig. 3E) and at least one order of magnitude on–off ratio, comparable to those of similar devices fabricated by electron-beam lithography (20). No hysteresis was observed by us during the electrical characterization of the transistors. The average transconductance at the source-drain voltage of –1.0 V and threshold gate voltage were found to be ~200 ± 80 nS (Fig. 3G), and ~7.0 ± 1.5 V, respectively (Fig. 3H). The dispersion of these device characteristics, as well as that of the on–off ratio (Fig. S5), could partly originate from the nonuniformity of the NW diameter (Fig. S6 and SI Results and Discussion). The calculated mobility and density of charge carriers were estimated to be 60 ± 30 cm²/Vs (Fig. S7) and 1.8 × 10¹⁹ ± 0.8 × 10¹⁹ cm−², respectively, consistent with previously reported data (20).

To demonstrate the self-integration of NWs into a complex multidevice circuit via guided growth, we have fabricated a tree address decoder made of 14 interconnected single-NW transistors (Fig. 4 A and B). The decoder selects one of 2ᴺ-bit lines in response to an input address of N bits (in our case N = 3). The input bit applied to each of the three transistor rows is defined as “1” when Aᵢ gate voltage turns the transistors on and Aᵢ gate voltage turns the transistors off. Similarly, the input bit is defined as “0” for the opposite combination. The performance of the decoder was characterized by applying a constant dc load of 5 V on each bit line separately, and gate voltages of 0 V and –5 V were applied to turn the transistors on and off, respectively, as the input signals. With average output signals of 2.9 ± 0.2 V and 0.58 ± 0.09 V for closed and opened bit lines, respectively (Fig. 4C), the decoder exhibits an average on–off ratio of 5 (see SI Results and Discussion for further details). These results demonstrate the feasibility of NW self-integration into electronic circuits via guided growth.

In summary, we have demonstrated the massively parallel self-integration of discrete NWs into circuits by guided growth from nanopatterned catalyst. The NW position accuracy, and the simplicity of the registration between NWs and electrodes, enables the realization of complex multidevice systems. This unique concept combines bottom-up and top-down fabrication approaches
into one fully parallel process, adopting the advantages of both. On the one hand, the bottom–up synthesis provides highly controlled nanostructures with unique electronic properties. On the other hand, the top–down fabrication used to produce the catalyst nanopattern offers the arbitrariness and long-range order of the nanostructure organization required for large-scale integration. The demonstrated high-throughput parallel fabrication of hundreds of single-NW electronic devices, as well as the realization of a multidevice integrated circuit, highlights the potential of our approach for NW-based nanoelectronics.

We used ZnO NWs grown on sapphire as a model system to prove this concept. However, recently reported alternative surface-guided growth systems, such as of GaN NWs on sapphire substrates (5) or GaAs NWs on GaAs substrates (30), show that this concept can be applied to a broad variety of NW materials and substrates. Further areas to study include (i) guided growth of NWs with coherently modulated composition and doping, allowing integration of p-type and n-type NWs, and heterojunctions (31); (ii) the transfer of the assembled NWs and circuits onto other substrates such as silicon and plastics (15) (Initial results have already been achieved by our group by selective etching of the substrate. These preliminary results already demonstrate that the guided growth approach is general and versatile and not limited to any specific materials or substrates.); and (iii) a better understanding of the guided growth mechanism. This will lead to further miniaturization of NW-based integrated circuits. This work presents a successful combination of parallel top–down and bottom–up processes potentially compatible with industrial technologies of lithography and chemical vapor deposition. This compatibility, together with the deterministic control of NW position, direction, and length, represents an important advantage with respect to postgrowth assembly processes. Thus, the demonstration of this self-integration concept opens a promising pathway toward the realistic application of NWs in large-scale functional systems.

**Materials and Methods**

**Catalyst Seed Nanopatterning and NW Growth.** R-plane sapphire substrates (Roditi International Ltd.) were patterned by electron-beam lithography (JEOL FS-9300) using a bilayer of 200K (100 nm)/PMMA (150 nm) Poly (methyl methacrylate) (PMMA) resist (Microresist Technology GmbH), following by Au electron-beam evaporation (1–5 nm) and liftoff in acetone. The Au pattern was dewetted by heating the substrates to 550 °C in air for 3 min. NW synthesis was carried out in a quartz tube, using ZnO mixed with carbon powder (1:1 wt/wt) as a precursor and N2 as a carrier gas, as previously reported (20). During the growth, the temperature at the precursor source was set to 1,000 °C, and the temperature at the target substrate was set to 850–900 °C.

**Nanoimprinted Catalyst Pattern.** We patterned 495 K PMMA film with a thickness of 100–150 nm on Si substrates by electron-beam lithography, and used them as masters for soft mold preparation. The hybrid soft h-PDMS/PDMS melds were prepared according to the procedure provided by Odom et al. (32). Sapphire substrates were first spin-coated with an adhesion layer of 495 K PMMA (50 nm) and baked at 180 °C for 2 min. UV-curable resist (NOA-61, Norland Products Inc.), diluted in Propylene glycol monomethyl ether acetate (PMGEA) to provide a thickness of 150–200 nm, was then applied by spin-coating, and the substrate was exposed under the UV lamp (365 nm, 10 mW/cm²) of Karl Suss MA-6 mask-aligner (33). Then the substrate
Fig. 4. NW-based three-bit address decoder. (A) Electronic scheme of three-level tree address decoder. To provide an example of the decoder operation, the scheme demonstrates the states of the transistors when the input level is 110. All of the colored transistors are in an “on” state, connecting B6 to the data line. (B) SEM of the NW decoder made of 14 interconnected single-NW field-effect transistors. (Scale bar, 6 μm.) Drain, source, and gate electrodes in the inset are signed by the letters D, S, and G, respectively. (C) Electrical characterization of the NW decoder. Each colored plot represents a manually measured output signal from one eight-bit line, as a function of the address input signal.

Device Fabrication by Photolithography. Source and drain electrodes were patterned using Shipley S1813 photoresist, electron-beam evaporation of Ti (20 nm)/Al (20 nm)/Pt (20 nm)/Au (20 nm) and liftoff in hot acetone. Al2O3 patterned using Shipley S1813 photoresist, electron-beam evaporation of Ti covers the resist surface, except the bottom parts of the imprinted features. Then, the resist was overetched by exposing the substrates to oxygen plasma (STS ASE ICP, 20 mTorr, 80 sccm of O2, coil power 200 W, platen power 50 W) through the Ti mask for 5 min. Finally, an Au film was deposited by electron-beam evaporation, followed by liftoff in hot (60 °C) N-methyl-pyrrolidone.

was brought in contact with the mold, slightly pressed to evacuate air traps from the mold-substrate interface, and UV-exposed through the mold for 15 min. Finally, the mold was gently separated from the substrate.

To prevent the widening of the imprinted features during the plasma etching of the resist residual layer, a Ti hard mask (45 nm) was electron-beam evaporated while the substrates are tilted by 30° (Fig. S6) (29). The angle-etching of the resist residual layer, a Ti hard mask (45 nm) was electron-beam evaporated while the substrates are tilted by 30° (Fig. S6) (29).

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Supporting Information

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SI Results and Discussion

Periodicity and Density of NW Arrays. In guided growth, the nanowire (NW) density is limited by the density of seed catalyst nanoparticles. Therefore, guided growth has not yet been able to yield close-packed NWs, as achieved by Langmuir–Blodgett assembly (1). Using continuous catalyst film, the seed nanoparticles are formed by thermal dewetting, and we obtained up to eight randomly positioned NWs per μm (2). We roughly estimate that for densities higher than ~10 NWs/μm, Ostwald ripening and Au surface mobility might limit the NW yield and positioning control. On the other hand, we believe that higher densities could in principle be achieved with smartly designed nanopatterned catalysts that pin the nanoparticles at staggered locations to avoid Ostwald ripening and Au surface mobility.

NW Diameter Statistics. The cross-section of horizontal ZnO NWs obtained by guided growth on R-plane sapphire is not perfectly circular, but has a flat base, and roughly a 1:1 base–height ratio (2). In this work, we estimated NW diameter from Atomic Force Microscopy (AFM) and measured NW height based on this geometry. The NW diameter statistically evaluated from three different growth batches had an average value of 8.5 ± 2.5 nm (Fig. S6), reaching its minimum at 5 nm. The NW diameter distribution probably originates from the catalyst nanoparticle size distribution, and is likely among the reasons for the variability in the device characteristics. We believe that more uniform catalyst nanoparticles can be achieved by improving deposition condition to get lower grain size of the catalyst film, as well as by optimizing the dewetting time.

NW Decoder. In this work, we presented a fully functional decoder, whose operation demands effective switching and uniform characteristics from all of its 14 transistors. This yield is seemingly higher than the 85% that was demonstrated for the massively parallel production of 100 single-NW transistors (Fig. 3). This could be attributed to the fact that this prototype circuit (Fig. 4) was produced by electron-beam lithography, which is generally characterized by higher nanoscale pattern fidelity. Similar fidelity can in principle be achieved in a massively parallel process, as in Fig. 3, with proper optimization. We also believe that the decoder characteristics, such as attenuation of the output voltage swing of ~30–50%, can be substantially improved by enhancing the transistor on–off ratio (3), mostly through the optimization of the device fabrication processes. Also, using high-mobility semiconductor nanowires (4, 5) can facilitate similar devices with the input and output signals in the same range essential for large-scale circuits, where the output of one logic device drives the input of another one.


Fig. S1. A typical array of catalytic seed nanodots on sapphire substrate produced by electron-beam lithography, Au evaporation, and liftoff. (Scale bar, 2 μm.)
**Fig. S2.** Array of 125 NWs used for statistical characterization of NW positioning accuracy. (Scale bar, 10 μm.)

**Fig. S3.** Catalyst patterning by nanoimprint lithography. (A) Schematic process flow of soft-mold replication from a Si/Poly (Methyl Methacrylate) (PMMA) master. The PMMA nanopattern defines the 3D mold structures. (B) Schematic process flow of the nanoimprint pattern transfer. The Ti angle-evaporated mask keeps the final dimension of the transferred pattern as defined by the imprint mold and enables easy and robust liftoff due to the undercut formed in the metal mask after the resist etching.

**Fig. S4.** Arrays of NWs grown from nanoimprinted Au catalysts, which were used for parallel fabrication of transistors. Each row contains 100 NWs grown in two opposite directions. (Scale bar, 40 μm.)
Fig. S5. Current on-off ratio distribution for the transistors produced by massively parallel fabrication. The ratio was defined as current \(V_g = 10\, \text{V}/\text{current} \quad (V_g = -10\, \text{V})\) at the source-drain voltage of \(-1.0\, \text{V}\).

Fig. S6. NW diameter distribution, estimated by AFM measurement of NW height.

Fig. S7. Field-effect mobility distribution calculated for the transistors produced by massively parallel fabrication. The calculation assumes single-wire transistor with an average diameter of 8.5 nm.