**σ-π** molecular dielectric multilayers for low-voltage organic thin-film transistors

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Contributed by Tobin J. Marks, February 7, 2005

Very thin (2.3–5.5 nm) self-assembled organic dielectric multilayers have been integrated into organic thin-film transistor structures to achieve sub-1-V operating characteristics. These new dielectrics are fabricated by means of layer-by-layer solution phase deposition of molecular silicon precursors, resulting in smooth, nanostructurally well defined, strongly adherent, thermally stable, virtually pinhole-free, organosiloxane thin films having exceptionally large electrical capacitances (up to ≈2,500 nF-cm⁻²), excellent insulating properties (leakage current densities as low as 10⁻⁹ A-cm⁻²), and single-layer dielectric constant (k) of ≈16. These 3D self-assembled multilayers enable organic thin-film transistor function at very low source-drain, gate, and threshold voltages (<1 V) and are compatible with a broad variety of vapor- or solution-deposited p- and n-channel organic semiconductors.

Organic thin-film transistors (OTFTs) based on π-electron materials are envisioned as critical components of future electronic technologies and would enable low-cost solution-processed/printed logic circuits, displays, and sensors (1–3). Of the two fundamental OTFT components, the semiconductor and the dielectric, the greatest research effort by far has focused on the organic semiconductor, with impressive results achieved in increasing carrier mobility, for both hole-transporting (p-type) (2–4) and electron-transporting (n-type) (2, 5, 6) semiconductors, and in developing low-cost fabrication processes (7–9). However, mobilities are still modest by inorganic semiconductor standards and transistor function at unacceptably high operating voltages (30–100 V), a serious impediment to useful technologies. A breakthrough would be to develop nanoscale, high-yield growth methodologies enabling state-of-the-art OTFT performance at drastically reduced operating voltages. We report here a successful realization of one such approach in which robust, 3D-crosslinked, self-assembled dielectrics are fabricated by means of layer-by-layer deposition of σ-π organosilane modules.

Typical “top-contact” OTFTs contain a semiconductor layer on top of a dielectric, together with an underlying gate electrode and top charge-injecting/extracting source and drain electrodes (Fig. 1). Current flowing between source and drain electrodes (I₉₈) on application of a drain-source bias (V₉₈) is minimal when zero voltage is applied between gate and drain electrodes (V₉ = 0), in which the device is “off.” However, as V₉ is increased in magnitude, charge carriers are accumulated at the semiconductor-dielectric interface, resulting in a gate-modulated I₉₈ (“on” state). Parameters characterizing thin-film transistor (TFT) performance include the field-effect mobility (μ), and the current on/off (I₀ᵣ/I₉₈) ratio, defining the drain-source current ratio between on and off states. I₉₈ in the linear regime (10) is then expressed by Eq. 1, where W and L are the TFT channel width and length, respectively (Fig. 1), V₉₈ is the threshold voltage, and C₉ is the dielectric capacitance per unit area (Eq. 2, where k is the dielectric constant, ε₀ is the vacuum permittivity, and d is the dielectric thickness).

\[ I_{DS} = \frac{W}{L} \mu C_{i} \left[ V_{G} - V_{T} - \frac{V_{DS}}{2} \right] V_{DS} \quad [1] \]

\[ C_{i} = \varepsilon_{0} k \quad [2] \]

Note that for a given device geometry and semiconductor, equivalent I₀ᵣ/I₉₈ ratios are achieved at lower operating biases by increasing C₉, which stabilizes the carrier density in the semiconductor channel. This C₉ effect on I₉₈ is important for OTFTs considering the modest μ values of organic semiconductors, which are typically <1 cm²V⁻¹s⁻¹ vs. 10³ cm²V⁻¹s⁻¹ for crystalline Si. Furthermore, high-quality ultrathin gate dielectrics will be essential in combination with small channel lengths for high frequency operation (11, 12) and self-assembled molecular electronics (refs. 13 and 14 and references therein).

Recent efforts to increase C₉ and to increase I₀ᵣ/I₉₈ have striven either to increase k or to reduce d while managing the aforementioned challenges, by using either self-assembled monolayers (SAMs) of monofunctional (15) and phenoxype-terminated (16) hydrocarbon chains or relatively thick sputtered films of conventional metal oxides having greater k than SiO₂, e.g., BaSr₄Ti₅O₁₉₅ (11), Ta₂O₅ (17), or TiO₂ (18). Ultrathin polymeric dielectrics fabricated by means of polymerization of self-assembled initiators (19) on the gate dielectric or crosslinking of conventional polymers with suitable silane reagents (M.-H.Y., unpublished data) are also promising approaches. As dielectrics, the high defect densities and fragility of simple alkyl SAMs result in low device yields and modest OTFT response, although terminal phenoxype functionalization, which is thought to enhance SAM packing and prevent semiconductor molecule intercalation (16), significantly improves pentacene TFT performance. The modular synthetic approach reported here utilizes 3D-crosslinked dielectric multilayers grown from solution by means of self-limiting sequential chemisorptive deposition of the following σ-π building blocks (Fig. 1): (i) α,ω-difunctionalized hydrocarbon chains (Alk) that transversely crosslink, enabling precise stepwise layer build-up, increasing interchain packing, and reducing defects/pinholes; (ii) highly polarizable “push–pull” stilbazolium layers (Stb) self-assembled into oriented π-electron layers that should stabilize charge carriers in the semiconducting channel, including bound and free charges (20); and (iii) octachlorotrisiloxane capping layers (Cap) that enhance multilayer structural robustness by capping/planarizing with a crosslinked, glassy siloxane polymer. The resulting OTFTs function in the sub1V bias regime and exhibit very low leakage currents over large gate electrode areas, very large breakdown fields, and excellent device characteristics.

Abbreviations: ITO, tin-doped indium oxide; SAM, self-assembled monolayer; MIS, metal-insulator-semiconductor; TFT, thin-film transistor; OTFT, organic TFT.

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were cleaned according to standard procedures (see Supporting Materials) and were dried at 110°C for 5 min. All self-assembly procedures were performed in an N2-filled glove bag. A scheme describing the self-assembly process is shown in Fig. 2.

**Materials and Methods**

**Materials and Self-Assembly Procedure.** Semiconductors 1–5 and Stb were available in our laboratory (see Supporting Materials, which is published as supporting information on the PNAS web site). Alk and Cap were purchased from Gelest (Morrisville, PA). All Si wafers and tin-doped indium oxide (ITO) substrates were cleaned according to standard procedures (see Supporting Materials) and were dried at 110°C for 5 min. All self-assembly procedures were performed in an N2-filled glove bag. A scheme describing the self-assembly process is shown in Fig. 2.

**Device Fabrication.** For OTFTs, semiconducting materials (1–4) were vacuum deposited at ≈2 × 10⁻⁶ torr (500 Å, 0.2 Ås⁻¹) while maintaining the substrate-nanodielectric temperature at 60°C. Films of 5 were deposited from a xylene solution (500 ppm) at 105°C. Gold electrodes for OTFT/metal–insulator–metal devices were vacuum-deposited through shadow masks at 3 × 10⁻⁶ torr to 4 × 10⁻⁶ torr (500–1000 Å, 0.5 Ås⁻¹).

**Electrical Measurements.** All OTFT measurements were carried out in air except for compound 3, which was measured in vacuum (8 × 10⁻⁵ torr) by using a Keithley 6430 Sub-Femtoamp Remote Source Meter and a Keithley 2400 source meter, operated by a local LABVIEW program and general purpose interface bus communication. Triaxial and/or coaxial shielding was incorporated into the measurement. A digital capacitance meter (Model 3000, GLK Instruments, San Diego) and impedance/gain-phase analyzer (S1260, Solartron Analytical, Hampshire, U.K.) were used for capacitance measurements.

**Results and Discussion**

To validate the modularity of this approach and to elucidate structure–function relationships, three nanodielectrics of incrementally varied structure and thickness were fabricated (Figs. 1 and 2). These nanodielectrics are identified by the following nomenclature: I (layers, Alk+Cap), II (layers, Stb+Cap), and III (layers, Alk+Cap+Stb+Cap). The microstructures, electrical properties, and responses of TFTs fabricated with I–III were characterized as reported below. The synchrotron x-ray reflectivity-derived thicknesses of the nanoscopic dielectrics are 2.3 (I), 3.2 (II), and 5.5 (III) nm (±10%). Optical absorption (see Fig. 6, which is published as supporting information on the PNAS web site) and optical second-harmonic generation measurements on II and III demonstrate net polar alignment of the Stb dipoles with an average molecular tilt angle of ≈40° from the surface normal, whereas atomic force microscopy and SEM images of I–III are featureless, with rms roughness approximately that of the Si substrate, 0.5–1.0 nm, and consistent with crack/pinhole-free morphologies. The excellent insulating properties of I–III are demonstrated by cyclic voltammetry (Fig. 3a) by using ferrocene probe solutions with either bare ITO-coated glass working electrodes or those coated with I–III. From the magnitude of the current at any potential, it can be seen that there is passivation of the ITO surface with respect to ferrocene oxidation/reduction as successive ultrathin dielectric layers are built up, arguing that these multilayers eliminate the majority of pinholes (potential short circuits), which would compromise OTFT performance. This conclusion is further confirmed by quantitative solid-state leakage current measurements through the nanodielectrics, made on MIS and metal–insulator–metal (ITO-based; see Supporting Materials) sandwich structures fabricated by thermal evaporation of 200 × 200 μm² Au contacts onto I–III (Fig. 3b). Although Si/Si native oxide substrates exhibit very large current densities of ≈0.1–1.0 A/cm² at 1.0 V, thin films of I, II, and III reduce the leakage currents by ≈6 and ≈9 orders of magnitude, respectively. Current densities of III (≈10⁻⁹ A/cm²) can be compared to reported SAM values spanning the broad range of 10⁻⁵ to 10⁻⁹ A/cm² for smaller area (100 × 100 μm²) Au contacts (21) to 10⁻⁹ to 10⁻⁵ A/cm² reported by others (15, 18, 19). The measured breakdown fields for I–III (5–7 MV/cm⁻¹) rival or exceed those reported for far thicker (≈50 nm) metal oxide (17) and polymer (ref. 14 and references therein) dielectric layers (0.1–5 MV/cm⁻¹), previously used in OTFTs.

![Diagram](image-url)

**Fig. 1.** Schematic representation of the components of an OTFT showing the molecular structures of various organic semiconductors (Left) and self-assembled nanodielectrics I–III (Right). Highly n-type doped Si (100) wafers with a 1.5-nm native oxide or smooth ITO (a transparent conductor) were used as substrate/gate electrodes. Nanodielectric layers were sequentially deposited from solutions of silane precursors Alk, Stb, or Cap. The OTFT device was completed by vacuum-deposition of 50-nm-thick layers of p- or n-type organic semiconductors 1–4 or solution-deposition of semiconductor 5, followed by source-drain gold electrode (100 nm) vacuum deposition.
III

Leakage current measurement for nanodielectrics

Fig. 3. Leakage current measurement for nanodielectrics I–III. (a) Film pinhole assay by cyclic voltammetry (current vs. voltage) by using ferrocene/ferrocenium⁻ solutions in tetrahydrofuran/tetrabutylammonium hexafluorophosphate (Ag pseudoreference electrode; Pt counter electrode) using bare ITO (dotted line) and nanodielectrics I–III coated ITO as working electrodes (solid line). Electrode areas were 0.5 cm². (b) Measured leakage current density J vs. voltage plots without (bare substrate) and with nanodielectrics I–III in MIS sandwich structures on n⁺-Si. As expected, the J–V curves are slightly asymmetric at ~0.0 V, reflecting the different nature of the Au-siloxane-insulator and n⁺-Si-native oxide-insulator interfaces.

Fig. 4. Capacitance/loss measurements for I–III in MIS structures for nanodielectrics I (red), II (blue), and III (black) of Fig. 1. (a) Measurement of nanodielectric capacitance–voltage electrical characteristics at 10 Hz (solid line is the forward scan; broken line is the return scan). (Inset) Equivalent circuit representation. Note that the contribution of the nanodielectric capacitor (C) component to the total circuit impedance predominates over the series (Rf) and parallel (Rs) resistances as well as over the estimated parasitic capacitance. (b) Frequency (f) dependence of the capacitance (solid lines) and loss (broken lines) in the accumulation regime (1 V) between 10² and 10⁴ Hz for the indicated nanodielectrics.

(I), C₁ = 710 (II), and C₁ = 390 (III) nF cm⁻² (±5%) at 10² Hz, with slight fall-off (~15%) at higher frequencies. These values are far greater than the capacitance of conventional 300-nm-thick SiO₂ dielectrics typically used for OTFTs (~10 nF cm⁻²), greater than our estimates for the best siloxane SAM (~150 nF cm⁻²) (24), and comparable to the highest reported for a metal oxide dielectric, C₁ = 150–750 nF cm⁻² for thicker (~50–100 nm) sputtered TiO₂ films (17). The nanodielectric loss factor (~10⁻¹ to 10⁻²) is greater than in optimized complementary metal oxide semiconductor SiO₂ dielectrics (~10⁻⁴) and, at all frequencies, I–III exhibit 0.1–0.4 V hystereses. However, annealing at 120–180°C reduces all hystereses to <0.1 V and reduces frequency-dependent C–V dispersion, suggesting that pristine I–III contain some quantities of fixed positive charges (Qf), ~2 × 10⁻² to 5 × 10⁻² cm⁻² (23, 24). Interface state densities (Df0) calculated from standard C–V and G–V (conductance–voltage) plots (25) are ~3 × 10⁻² cm⁻¹ cm⁻² (1 eV = 1.602 × 10⁻¹⁹ J). Importantly, annealing reduces Qf and Df to ~10¹¹ cm⁻² and ~10¹² eV⁻¹ cm⁻², respectively, which are near standard values for SiO₂ and many high-k dielectrics (22).

Also important are the magnitudes of the effective dielectric constants [k_eff = (C₁ · d_I−III)/ε₀, Eq. 2] achieved in I–III, which are the best estimated by measuring C₁ in metal-insulator-metal structures (see Fig. 7, which is published as supporting information on the PNAS web site). Note that the presence of the Si-SiO₂ interface strongly limits the maximum charge storage in the accumulation layer resulting in underestimated C₁ values (24). If the contributions of individual Alk and Stb organic layers (δorg) are estimated by pragmatically assuming parallel-plate capacitors of thickness d_{I−III} = d_{org} + d_{cap} in series (Eq. 3) with Cap forming a SiO₂ network (d_{cap} = 0.83 ± 0.1 nm by x-ray reflectivity) (26), then k_eff of I and II can be approximated by multilayers composed of Alk and Stb monolayers and oxide layer (k_{org} ~ 3.9) (10).

\[
\frac{d_{I−III}}{k_{eff}} = \frac{d_{org}}{k_{org}} + \frac{d_{cap}}{k_{cap}}
\]

From the maximum metal–insulator–metal capacitance values [C₁ = 1,100 (I), 2,500 (II), and 760 (III) nF cm⁻² (2.5%)], k_{org}

\[\text{[3]}
\]

When the C–V transition from inversion to accumulation is sharp with small changes in the depletion C–V slope with frequency (no “stretch-out”), interface trap contributions are generally ignored (they cannot follow the ac voltage at high frequencies), and fixed charge density can be estimated from Qf = CA_{Vfb} where \(A_{Vfb} = [V_{fb}(10^5 \text{ Hz})] - V_{fb}(10^2 \text{ Hz})\).

From published data (24), we estimate k < 1 (nonphysical) for a number of simple alkyl SAM grown on Si-native oxide substrates.

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of the Alk and Stb layers is estimated to be ~2.5 (close to that of bulk paraffins and alkyl SAMs) (27) and ~16, respectively. This result illustrates the strategic importance for this and future work of highly π-polarizable dipolar layers in enhancing \( k_{eff} \), hence increasing \( C \), while preserving excellent insulator properties.

OTFTs (Fig. 1; \( L = 100 \mu m, W = 5 \text{ mm} \)) were next fabricated on I–III, with all devices exhibiting reproducible \( I-V \) characteristics at low biases with classical linear and saturation response (10), as exemplified with typical p-type (I) and n-type (4) semiconductors (Fig. 5). Note that the operation window can be enlarged substantially by substituting multilayer III for II/I (Fig. 5b), because of the increased breakdown resistance, in agreement with the aforementioned leakage current data. Similar transistor characteristics are obtained for a range of vapor/ solution-deposited organic semiconductors, demonstrating broad generality. In marked contrast, control devices fabricated with a thicker SiO\(_2\) dielectric require far larger operating voltages for useful \( I_{DS} \) (Fig. 5a Inset).

Nanodielectric III was next evaluated extensively in TFT geometries. Typical laboratory scale device fabrication yields were >98%. Table 1 summarizes data for semiconductors 1–5 (operating biases 0.0 to ±1.0 V) and for comparison, those using standard 300-nm SiO\(_2\) as the gate dielectric (operating biases 0 to ±100 V). Note that comparable \( \mu \) values are now obtained at far smaller operating biases and that \( V_{th} \)s are now only fractions of volts. The \( I_{off}/I_{on} \) ratios should be further enhanced with second-generation device configurations and by more elaborate patterning of the semiconductor (28). Note also that OTFTs fabricated on glass-coated ITO gates function comparably, demonstrating that a Si/Si native oxide gate is not required to achieve excellent performance (Fig. 5d and see also Fig. 8, which is published as supporting information on the PNAS web site) and that optically transparent low-voltage devices are readily fabricated. These nanodielectrics also can be used to fabricate flexible OTFTs on commercially available plastic (Mylar)-coated ITO gates (see Fig. 9, which is published as supporting information on the PNAS web site), demonstrating applicability to transparent flexible plastic electronics. Finally, note that the thermal stability of the new nanodielectrics (74°C < 200–300°C) suggests compatibility with inorganic semiconductors that can be deposited at such low temperatures.

### Conclusions

The aforementioned results demonstrate that designed self-assembling building blocks incorporating extensive 3D crosslinking and π-electron constituents enable precise, solution phase fabrication of extremely thin, nanostructurally ordered, pinhole-free, high-capacitance/high-\( k \)/low leakage organic multilayer dielectrics. These molecule-derived 2.3- to 5.5-nm-thick dielectrics can be efficiently integrated into large-area p- and n-channel OTFTs (single TFT area ~10\(^2\) nm\(^2\)) demonstrating great uniformity with a variety of substrates. The results argue that many of the charge transporting limitations of current organic semiconductors can be circumvented and that this assembly methodology combined with other crosslinkable high-\( k \) π-electron modules should be adaptable to creating even higher dielectric constant and higher capacitance molecular multilayers.

We thank Prof. P. Dutta and Dr. C. Yu for helpful discussions. This work was supported by the National Aeronautics and Space Administration Institute for Nanoelectronics and Computing, the Motorola Technology Center, the Office of Naval Research, and the National Science Foundation—Materials Research Science and Engineering Center program through the Northwestern Materials Research Center.

### Table 1. Field effect transistor data for organic semiconductors 1–5 using the nanodielectric III on n-type Si substrates

<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>( \mu, \text{cm}^2\text{V}^{-1}\text{s}^{-1} )</th>
<th>( I_{off}/I_{on} )</th>
<th>( V_{th}, \text{V} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.06 (0.04)</td>
<td>7 × 10(^2) (10(^4))</td>
<td>0.08 (–4)</td>
</tr>
<tr>
<td>II</td>
<td>0.07 (0.03)</td>
<td>6 × 10(^2)</td>
<td>0.05</td>
</tr>
<tr>
<td>2</td>
<td>0.02</td>
<td>1 × 10(^3)</td>
<td>0.06</td>
</tr>
<tr>
<td>3</td>
<td>0.04</td>
<td>8 × 10(^2)</td>
<td>0.03</td>
</tr>
<tr>
<td>4</td>
<td>0.002 (0.02)</td>
<td>5 × 10(^2) (10(^4))</td>
<td>−0.17 (2)</td>
</tr>
<tr>
<td>5</td>
<td>0.02 (0.2)</td>
<td>6 × 10(^2) (10(^4))</td>
<td>0.21 (14)</td>
</tr>
<tr>
<td>6</td>
<td>0.003 (0.001)</td>
<td>3 × 10(^2) (10(^4))</td>
<td>−0.22 (20)</td>
</tr>
<tr>
<td>7</td>
<td>0.01 (0.02)</td>
<td>2 × 10(^2)</td>
<td>−0.20 (–40)</td>
</tr>
</tbody>
</table>

Operating biases were 0.0 to ±1.0 V. Data in parentheses are for 300-nm-thick SiO\(_2\) dielectric devices. All TFT mobilities (\( \mu \)) and threshold voltages (\( V_{th} \)) are calculated in the saturation regime (11).

*Calculated at \( V_G = 0.0 \) to ±1.0 V (0 to ±100 V) and \( V_{DS} = ±1.0 \) V (±100 V).
†Data for nanodielectric III on glass-ITO substrates.

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