Deposition of high-κ dielectrics onto graphene is of significant challenge due to the difficulties of nucleating high quality oxide on pristine graphene without introducing defects into the monolayer of carbon lattice. Previous efforts to deposit high-κ dielectrics on graphene often resulted in significant degradation in carrier mobility. Here we report an entirely new strategy to integrate high-quality high-κ dielectrics with graphene by first synthesizing free-standing high-κ oxide nanoribbons at high temperature and then transferring them onto graphene at room temperature. We show that single crystalline Al₂O₃ nanoribbons can be synthesized with excellent dielectric properties. Using such nanoribbons as the gate dielectrics, we have demonstrated top-gated graphene transistors with the highest carrier mobility (up to 23,600 cm²/V·s) reported to date, and a more than 10-fold increase in transconductance compared to the back-gated devices. This method opens a new avenue to integrate high-κ dielectrics on graphene with the preservation of the pristine nature of graphene and high carrier mobility, representing an important step forward to high-performance graphene electronics.

Results and Discussion

Fig. 1 illustrates our approach to fabricate top-gated graphene transistors. Mechanically peeled graphene flakes on silicon substrate were used as the starting materials in initial studies, although the approach described here can be readily extended to graphene obtained through chemical exfoliation or chemical vapor deposition. Al₂O₃ nanoribbons were aligned on top of the graphene through a physical dry transfer process (Materials and Methods), followed by e-beam lithography and metallization process to define the source and drain electrodes (Fig. 1A). Oxygen plasma etch was then used to remove the exposed graphene, leaving only the graphene protected underneath the dielectric nanoribbon and the source drain electrodes (Fig. 1B). The top-gate electrode was then fabricated (Fig. 1C). A typical device consists of source, drain and top-gate electrodes (Ti/Au, 50 nm/50 nm), Al₂O₃ nanoribbon as the top-gate dielectric, a highly doped p-type silicon substrate (≈0.004 ohm·cm) as the back gate, and a 300 nm thermal silicon oxide layer as the back-gate dielectric.

Aluminum oxide, with a dielectric constant of 9.1, is an important high-κ material with excellent dielectric properties, thermal
and chemical stability (30). In our studies, Al₂O₃ nanoribbons were used as an example to demonstrate our concept of using preformed free-standing nanoribbons as the top-gate dielectrics. Al₂O₃ nanoribbons were synthesized through a physical vapor transport approach at 1400 °C (Materials and Methods). Transmission electron microscope (TEM) studies show that the Al₂O₃ nanoribbons typically have a width of 1–3 μm, and a length on the order of 10 μm (Fig. 2A). Selected area electron diffraction (SAED) study shows the nanoribbon has a single crystalline α-Al₂O₃ structure, oriented along (110) direction in its long axis, and along (001) direction (c-plane) in its thickness (Fig. 2A and Inset). The high resolution TEM (HRTEM) image confirms that the nanoribbon is a single crystal with nearly perfect crystalline structure free of any obvious defects (Fig. 2B). Atomic force microscopy (AFM) studies show that the nanoribbons typically have a thickness around 15–30 nm (Fig. 2C), and nearly atomically smooth surface with root mean square roughness <0.2 nm (Fig. 2D).

To understand the intrinsic dielectric properties of the nanoribbons, we have fabricated metal-insulator-metal (MIM) devices (Fig. 2E) to characterize the current tunnelling, breakdown, and dielectric characteristics. Electrical measurements of the MIM device show that current density (J) vs. electric field (E) relation exhibits typical Fowler–Nordheim (F–N) tunnelling behavior with a breakdown field of 8.5 MV/cm (Fig. 2F and Inset), comparable to the best quality ALD Al₂O₃ film (31). This type of field-assisted tunnelling can be described by charge carrier tunnelling through a triangular barrier with

\[ J = AE_{OX}^2 \exp(-B/E_{OX}) \]

where

\[ A = 1.54 \times 10^{-6} \left( \frac{1}{m^* \Phi_B} \right) \]

and

\[ B = 6.83 \times 10^7 \left( \frac{m^*}{\Phi_B} \right)^{1/2} \left( \frac{\Phi_B}{\Phi_0} \right)^{3/2} \]

J is current density, \( E_{Ox} \) is the oxide electric field, and \( m^* \) is the effective mass of the charge carrier, which is about 0.23 mₑ, and \( \Phi_B \) is the barrier height (31). Fitting the J – E characteristics with the F–N tunnelling model gives a tunnel barrier of about 2.0 eV between Al₂O₃ and Ti, comparable to previous reports of the barrier height between ALD Al₂O₃ and metals of similar work function (31, 32). The relative dielectric constant is also determined from capacitance-voltage measurement as 8.5, which is larger than typical values observed in ALD Al₂O₃ films (31). These studies clearly demonstrate that the Al₂O₃ nanoribbons have dielectric properties comparable to or better than the best quality ALD Al₂O₃ film (31), and can function as an excellent dielectric material for top-gated graphene transistors.

The Al₂O₃ nanoribbons can be aligned onto the top of the graphene through a physical transfer process (Materials and Methods). Previous studies have shown that the deposition of oxide on top of graphene often introduces significant defects into the graphene structure with an obvious defect band (D-band) emerging around 1350 cm⁻¹ in Raman spectra. To this end, we have employed micro-Raman spectroscopy to investigate the interaction between an Al₂O₃ nanoribbon and the underlying graphene (Fig. 3A and Inset). Micro-Raman spectra were
collected from bare graphene (Point a) and Al$_2$O$_3$ nanoribbon covered graphene (Point b). Significantly, there is no clear difference between two Raman spectra and there is no obvious D-band (Fig. 3A), in contrast to previous studies where an obvious D-band is observed (33).

The excellent dielectric properties observed in the single crystalline α-Al$_2$O$_3$ nanoribbons readily allows us to employ them as the gate dielectrics for top-gated graphene transistors (Fig. 3B and Inset). Cross-section TEM was used to study the graphene–dielectric interface (Fig. 3B and C). The gate stack (SiO$_2$/graphene/Al$_2$O$_3$/Ti/Au) could be observed in Fig. 3B. The HRTEM image of the device shows that the graphene layers are intimately integrated with the crystalline Al$_2$O$_3$ nanoribbon without any obvious gap or impurities between them (Fig. 3C).

Together, these studies clearly demonstrate that the physical assembly approach can effectively integrate Al$_2$O$_3$ nanoribbon with graphene without introducing any appreciable defects into the graphene lattice, and thus can effectively preserve the high carrier mobility in the resulting devices.

The electrical transport studies of the top-gated graphene transistors were carried out at room temperature. Fig. 4A shows the drain-source current ($I_{ds}$) versus drain-source voltage ($V_{ds}$) output characteristics of the transistor at various top-gate voltage ($V_{TG}$) of −1.5, −1.0, −0.5, 0.0, and 0.5 V. The device delivers an on current of 675 μA at $V_{ds} = 1$ V and $V_g = −1.5$ V. To evaluate the top-gated devices versus standard back-gated devices, we have measured the transfer characteristics, $I_{ds}$ versus top-gated voltage ($V_{TG}$) and back-gated voltage ($V_{BG}$) (Fig. 4B and Inset). Significantly, the required gate voltage swing to achieve similar current modulation in top-gate configuration is >1 order of magnitude smaller than that in back-gate configuration. The transconductance $g_m = \frac{\partial I_{ds}}{\partial V_{TG}}$ can be extracted from the $I_{ds}$–$V_{TG}$ curve (Fig. 4C). At $V_{ds} = 1$ V, the top-gated device exhibits a max $g_m$ of about 290 μS, which is about 15 times larger than that of the back-gated configuration ($g_m \approx 19.5$ μS).

Fig. 4D further shows two-dimensional plot of the device conductance as a function of varying $V_{BG}$ and $V_{TG}$ bias, from which we can determine the top-gate Dirac point ($V_{TGDirac}$) shift as a function of $V_{BG}$ (Fig. 4E). It gives the ratio between top-gate and back-gate capacitances, $C_{TG}/C_{BG} \approx 14.3$. This gate capacitance ratio is consistent with the improvement factor (approximately 15) in transconductance of top- versus back-gated configurations. Using the back-gate capacitance value of $C_{BG} = 11.5$ nF/cm$^2$, the top-gate capacitance is estimated to be $C_{TG} = 164.5$ nF/cm$^2$, corresponding to a relative dielectric

![Fig. 3](image_url) Characterization of the graphene/Al$_2$O$_3$ nanoribbon interface. (A) Raman spectra of the graphene with (Point b) and without (Point a) Al$_2$O$_3$ nanoribbon covering. The inset shows the optical image of an Al$_2$O$_3$ nanoribbon on graphene, the scale bar is 2 μm. There is no D-band in either spectrum, indicating that Al$_2$O$_3$ nanoribbon does not introduce any appreciable defects into graphene lattice. (B) A cross-section TEM image of the top-gate stack, the scale bar is 100 nm. The inset shows an SEM image of a typical device, the scale bar indicates 5 μm. The dotted line in the inset shows the cross-section cutting direction. (C) A cross-section HRTEM image of the interface between Al$_2$O$_3$ nanoribbon and a trilayer graphene. The partially incomplete graphene layers in the image are caused by electron-beam damage during the TEM imaging process.

![Fig. 4](image_url) Room temperature electrical properties of the top-gated graphene device using Al$_2$O$_3$ nanoribbon as the gate dielectric. (A) $I_{ds}$–$V_{ds}$ output characteristics, the channel width and length of the device is 2.1 μm and 4.1 μm. (B) Transfer characteristics at $V_{ds} = 1$ V for the device using top and back gate (Inset). (C) Transconductance $g_m$ as a function of top-gate voltage $V_{TG}$, the inset shows the $g_m$ vs. $V_{BG}$. The plots indicate the top gate $g_m$ is about 15 times higher than the back-gate $g_m$. (D) Two-dimensional plot of the device conductance at varying $V_{BG}$ and $V_{TG}$ bias. The unit in the color scale is μS. (E) The top-gate Dirac point $V_{TGDirac}$ at different $V_{BG}$. (F) Experimental plot (Black Line) and modeling fitting (Red Line) of $R_{tot}$ vs. $V_{TG}$–$V_{TGDirac}$ relation to derive the contact resistance and carrier mobility.
constant of 8.4 for Al₂O₃ nanoribbon, which is also consistent with the value obtained from MIM devices.

To further gauge the transistor performance, it is important to determine the carrier mobility. To accurately derive the mobility value, it is necessary to exclude the contact resistance that is comparable to the graphene transistor channel resistance. The total resistance of the device can be expressed as the following (25):

$$ R_{\text{tot}} = R_{\text{contact}} + R_{\text{channel}} = R_{\text{contact}} + \frac{L/W}{\mu n} $$  \[4\]

Where $R_{\text{channel}}$ is the resistance of the graphene channel covered by top-gate electrode, the contact resistance $R_{\text{contact}}$ consists of the uncovered graphene section resistance and the metal/graphene contact resistance, $L$ is the channel length, $W$ is the channel width, and $n$ is the carrier concentration in the graphene channel region, and can be approximated by the following equation

$$ n = \sqrt{n_0^2 + n_{\text{TG}}^2} = \sqrt{n_0^2 + \left(\frac{C_{\text{TG}}(V_{\text{TG}} - V_{\text{Dirac}})}{e}\right)^2} $$  \[5\]

where $n_0$ is the residual carrier concentration, representing the density of carriers at Dirac point (34); $n_{\text{TG}} = C_{\text{TG}}(V_{\text{TG}} - V_{\text{Dirac}})/e$ is the carrier concentration induced by the top-gate bias away from the Dirac point, $C_{\text{TG}}$ can be approximated by the oxide capacitance of 164.5 nF cm⁻² (the quantum capacitance is neglected here as it is >1 order of magnitude larger approximately 2000 nF cm⁻²).

By fitting this model to the measured data in Fig. 4B, we can extract the relevant parameters, $n_0$, $R_{\text{contact}}$, and $\mu$. Fig. 4F shows the measured $R_{\text{tot}}$ versus $V_{\text{TG}}$ (Black Line), along with the fitted curve derived from Eq. 4 (Red Line). The fitted curve agrees well with the experimental data, with a single value of the residual concentration $n_0 = 4.1 \times 10^{11}$ cm⁻², $R_{\text{contact}} = 1240 \Omega$, and the mobility $\mu = 22,400$ cm²/V · s, which represents the highest carrier mobility value observed in top-gated graphene devices to date. The fitted contact resistance $R_{\text{contact}} = 1240 \Omega$ is comparable to the $R_{\text{contact}}$ determined by four-probe measurements of similar devices (Fig. S1).

The mobility value derived from top-gated configuration is also consistent with that obtained from back-gated measurement (25,600 cm²/V · s). We have studied multiple devices fabricated with the same approach, all of which exhibited carrier mobilities well exceeding 10,000 cm²/V · s (Table 1), comparable to the best reported values in back-gated devices and about one order of magnitude better than typical values previously reported for top-gated devices (17, 20, 21). The variation in mobility values is commonly seen in graphene-based devices (35), which may be attributed to variable local environment with different local potential, defects, impurities, or stress. Together, these studies clearly demonstrate that the presence of Al₂O₃ nanoribbon on top of graphene does not lead to any mobility degradation, in contrast to previous efforts in using ALD or PVD to deposit dielectrics on graphene.

<table>
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<tr>
<th>Device No.</th>
<th>Thickness (nm)</th>
<th>Mobility (cm²/V · s)</th>
</tr>
</thead>
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<td>38</td>
<td>23600</td>
</tr>
<tr>
<td>2</td>
<td>45</td>
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Materials and Methods

Synthesis of Al₂O₃ Nanoribbons. Aluminum oxide (Al₂O₃) nanoribbons were synthesized through a physical vapor transport approach at 1400 °C. To grow Al₂O₃ nanoribbons, aluminum, and nanometer-sized Al₂O₃ powders with a molar ratio of 4:1 were used as the starting materials. The ceramic boat with the mixture was placed at the center of a horizontal tube furnace and an alumina piece was placed at the downstream as the deposition substrate. The temperature was raised to target temperature with a flow of 400 sccm Ar as the carrying gas. The temperature was maintained for 1 h and then naturally cooled to the room temperature.

Dry Transfer of Al₂O₃ Nanoribbons. The overall process involves physical transfer of Al₂O₃ nanoribbons directly from a Al₂O₃ nanoribbon growth substrate to a graphene substrate via contact printing. Specifically, a graphene device substrate is first firmly attached to a benchtop, and the Al₂O₃ nanoribbon growth substrate is placed upside down on top of the graphene substrate so that the Al₂O₃ nanoribbons are in contact with the graphene. A gentle manual pressure is then applied from the top followed by slightly sliding the growth substrate. The Al₂O₃ nanoribbons are aligned by shear forces during the sliding process. The sliding process results in direct dry transfer of nanoribbons from the growth substrate to the desired graphene substrate. The sample is then rinsed with isopropanol followed by nitrogen blow-dry, in which the capillary drying process near the Al₂O₃ nanoribbons can help the Al₂O₃ nanoribbons to be firmly attached to the substrate.

Characterization of Al₂O₃ Nanoribbons, Device Fabrication, and Measurements. The microstructures and morphologies of the Al₂O₃ nanoribbons were characterized by a JEOL 6700 SEM. The lattice image of the Al₂O₃ nanoribbons was observed by a FEI Titan HRTEM. The thickness was measured using atomic force microscope (AFM, Veeco Dimension 5000). Oxygen plasma (Diener Electronic) was used to selectively etch away the unprotected graphene region and leave graphene ribbons underneath the Al₂O₃ nanoribbon mask protection. The etch time is about 160 s at a power level of 40 W. The electrical transport properties were measured by a Lakeshore probe station with home built data acquisition system.


Table 1. The mobility values observed in multiple top-gate graphene transistors with variable Al₂O₃ thickness.

ACKNOWLEDGMENTS. We acknowledge the Electron Imaging Center for Nanomachines at the University of California Los Angeles for the technical support of TEM, Nanoelectronics Research Facility at the University of California Los Angeles for technical support of device fabrication. This work was supported by the Henry Samueli School of Engineering and an Applied Science Fellowship (Y.H.), and by the National Institutes of Health Director’s New Innovator Award Program, part of the National Institutes of Health Roadmap for Medical Research Grant 1DP2OD004342-01 (X.D.).


