Tuning the threshold voltage in electrolyte-gated organic field-effect transistors

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Low-voltage organic field-effect transistors (OFETs) promise for low power consumption logic circuits. To enhance the efficiency of the logic circuits, the control of the threshold voltage of the transistors are based on is crucial. We report the systematic control of the threshold voltage of electrolyte-gated OFETs by using various gate metals. The influence of the work function of the metal is investigated in metal-electrolyte-organic semiconductor diodes and electrolyte-gated OFETs. A good correlation is found between the flat-band potential and the threshold voltage. The possibility to tune the threshold voltage over half the potential range applied and to obtain depletion-like (positive threshold voltage) and enhancement (negative threshold voltage) transistors is of great interest when integrating these transistors in logic circuits. The combination of a depletion-like and enhancement transistor leads to a clear improvement of the noise margins in depleted-load unipolar inverters.

organic electronics | polyelectrolytes | thin-film transistors | gate electrode material

The possibility to process organic electronic materials from solution allows for printing electronic systems on a wide variety of large area and flexible substrates thus enabling new applications and ultralow cost electronics (1–3). The transistor is a corner stone in modern electronics. The OFETs are promising devices for applications that require medium-speed operation such as driving circuits for displays (4) and sensors (5, 6); however, to enable their integration in portable devices or electronic labels, i.e., distributed systems typically driven by printed batteries (7) or solar cells (8), the OFETs should operate at low voltage and power. A low driving voltage can be achieved by employing a gate dielectric composed of a ultrathin, cross-linked polymer (9), a self-assembled monolayer in combination with a thin metal oxide layer (10), or high-permittivity dielectrics (11); however, high-quality inorganic dielectrics or ultrathin organic dielectrics are normally difficult to combine with common printing technologies. Recently, various electrolytes have successfully been explored as the gate insulator in low-voltage operating OFETs (12–17). In this case, the formation of the gate capacitance includes polarization of electronic and ionic charges. Indeed, if we consider a p-channel OFET, applying a negative voltage to the gate attracts cations from the solution towards the electrolyte/gate interface while anions are repelled towards the electrolyte/semiconductor interface. Such ion redistribution results in the formation of electrical double layers (EDLs) at the two interfaces. These two EDLs can be assimilated to two capacitors in series in which the redistributed ions in the electrolyte are balanced by oppositely charged electronic charge carriers at the gate electrode and in the semiconductor, respectively (Fig. 1*A*). The ionic and electronic charges within these EDLs are separated by only a few Å resulting in a very high capacitance (typically above 1 μFcm^{-2}) that allows OFETs to operate below 1 V; however, one major drawback of using an electrolyte as the gate insulator material is that the switching speed is reduced. This is a result of the slow ion polarization within the electrolyte; however, polyelectrolyte-gated OFETs exhibit relatively fast switching speed (about 10 μs for short-channel devices) (18) and can be integrated into circuits with delay times of 300 μs (19).

One of the most important device parameters in field-effect transistors is the threshold voltage V_{TH}, which marks the gate voltage where a conducting channel forms between the source and drain electrodes. The corresponding energy diagram is shown in the *bottom* of Fig. 1*B*. Because organic semiconductors used in OFETs are nonintentionally doped, only two regimes can be found at both sides of the flat-band voltage V_{FB} that corresponds to the gate voltage V_{GS} where bands are flat all over the semiconductor layer. The two regimes correspond to *electron accumulation* when $V_{GS} > V_{FB}$ and *hole accumulation* when $V_{GS} < V_{FB}$; however, the existence of both of these regimes is actually constrained by the possibility to inject the appropriate charge carriers from the source electrode. Because gold is unlikely to inject electrons in P3HT due to a too high-energy barrier, the electron accumulation regime is replaced by a regime where the semiconductor layer behaves as a dielectric. For this reason, the regime at $V_{GS} > V_{FB}$ will be termed "dielectric" and is illustrated by a linear variation of the electric potential (constant electric field) across the film. The hole accumulation regime is marked by a small bend bending at the insulator-semiconductor interface that mirrors the accumulation of free charges there.

The flat-band potential can be estimated by measuring the photo potential as a function of the intensity of light illumination or the onset of the photocurrent. Its value is given by Eq. **1** where W_M and W_s are the gate and semiconductor work functions, respectively. q is the elementary charge, Q_{is} is the interface charge density, and C_i is the capacitance of the insulator layer (per unit area).

$$V_{FB} = \frac{W_M - W_S}{q} - \frac{Q_{is}}{C_i} \quad [1]$$

An additional difference between the flat-band and threshold voltages stems from an energy distribution of localized levels near the transport band edge that act as shallow traps for charge carriers (20–22). As the gate voltage increases, the traps become filled, and the charge carriers start to drift in the transport band.

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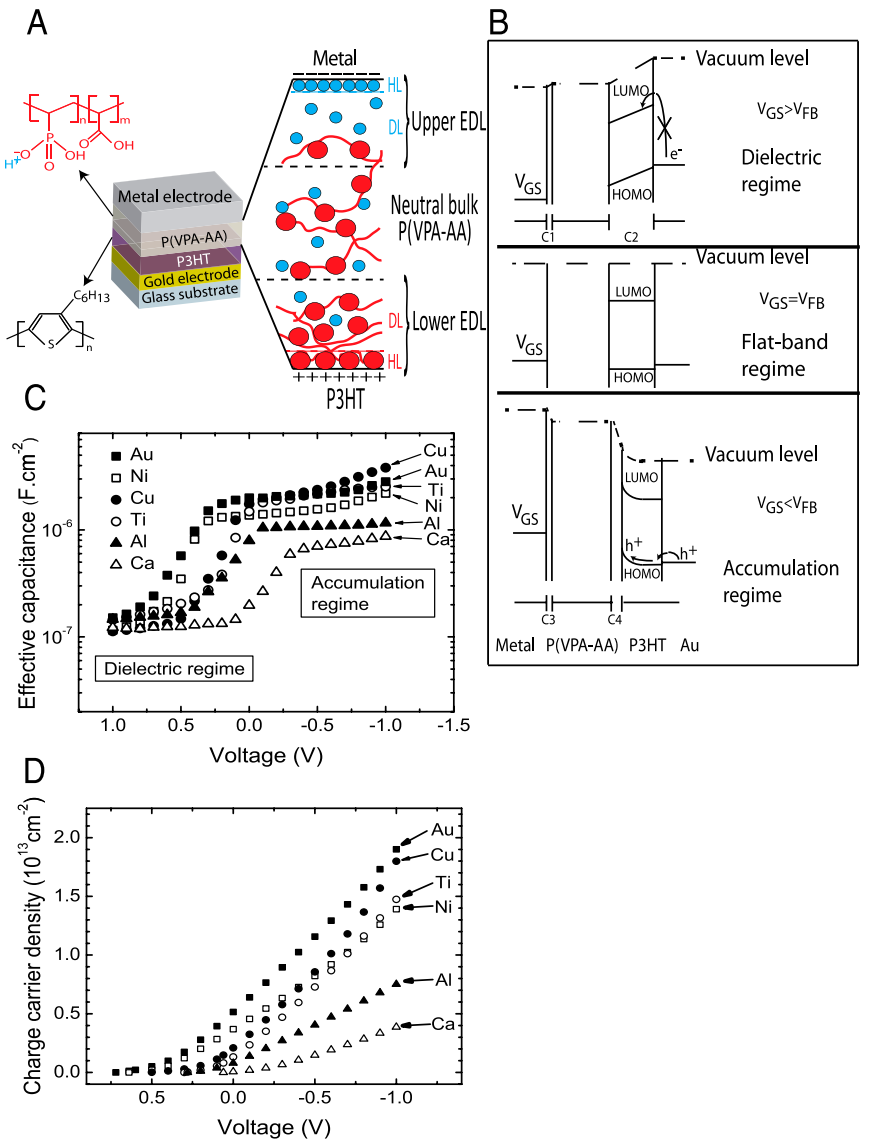

Fig. 1. Metal-Electrolyte-Semiconductor diode. (*A*) Schematic cross-section of the MES diode with the chemical formulae of P3HT and P(VPA-AA) and a schematic representation of charge distribution in the system capacitor. The red features represent the polyanionic chains and the blue circles the mobile protons. (*B*) Energy diagram of the different regimes of a metal-insulator-semiconductor stack. (*C*) Plot of the effective capacitance as a function of the voltage for six metals: Au (full squares), Ni (open squares), Cu (full circles), Ti (open circles), Al (full triangles), and Ca (open triangles). (*D*) Variation of the charge carrier density as a function of the gate voltage.

Ways to adjust the threshold voltage include the use of a second gate electrode (23) modifying the insulator-semiconductor interface with dipolar molecules (24) and doping the semiconductor (25). Furthermore, recent reports show that changing the gate electrode material may lead to a slight shift of V_{TH} (26).

In this paper, we report on a systematic control of V_{TH} in polyelectrolyte-gated OFETs by changing the metal of the gate. Because the operating voltage in these devices is comparable to the respective variation of the work function, it is possible to tune the threshold voltage over the whole potential window by changing the metal of the gate. In addition, we use the concept of V_{TH}-tuning to optimize the transition regime in depleted-load logic inverters.

Results and Discussion

Metal-Electrolyte-Organic Semiconductor Diodes. According to Eq. **1**, the flat-band potential linearly depends on the work function of the gate. The work functions usually found in tables are measured in high vacuum in order to avoid any surface contamination. In our devices, the gate consists of a metal film evaporated on top of the polyelectrolyte resulting in unavoidable degradations of the metal surface and subsequent modifications of the work function. Furthermore, the geometry of the device prevents any direct estimation of the actual work function, e.g., photoelectron spectroscopy or Kelvin probe measurements. Instead, we conducted capacitance-voltage measurements on capacitors made by stacking P3HT and the polyelectrolyte P(VPA-AA) between two metal electrodes (Fig. 1*A*). In all cases, the bottom electrode is made of gold. The effective area of the diode was 0.04 mm^2. The capacitance of the diode was measured as a function of the applied voltage at a frequency of 1 kHz. The curves in Fig. 1*C*, which represent the data for six different metals (i.e., gold, nickel, copper, titanium, aluminum, and calcium) behave differently from what is usually found in conventional semiconductor diodes where the voltage-dependent capacitance is explained in terms of modulation of a space-charge layer (27). Instead, the capacitance remains independent of the voltage up to a point where it abruptly increases to reach a second, higher

gate-voltage independent value. We explain this shape in terms of the model depicted in Fig. 1*B* that was detailed above. In the first regime, which corresponds to $V_{GS} > V_{FB}$, the semiconductor layer behaves as a dielectric because electrons cannot be injected from gold. Furthermore, proton penetration into the semiconductor bulk is unlikely due to the hydrophobicity of P3HT. This is confirmed with our capacitance measurement *SI Text*. Accordingly, we have two capacitances (C1 and C2) in series. Because the P3HT layer is thicker than the electrical double-layer at the metal electrode, its respective capacitance is lower. When two capacitances are in series, the total capacitance is dominated by the smallest one, C2 in that case. We note that the value of the capacitance in this voltage range is in line with that of the P3HT layer (*ca.* 0.1 μF/cm^2 for a 30 nm thick layer with a dielectric constant of 3). Below V_{FB}, accumulation of holes takes place and the P3HT film becomes conductive, so that the total capacitance reflects the double layers that form at the electrolyte-semiconductor interface (capacitor C4). Note that because metal-electrolyte C4 and semiconductor-electrolyte double-layer C3 capacitances have identical area, the presence of a thin-oxide layer at the surface of reactive metals (Ca, Al, and Ni) might lead to a situation where $C3 < C4$, which could explain the deviation of the measured capacitance compared to the other metals (Au, Cu, and Ti).

Based on this model, the flat-band voltage V_{FB} can be estimated as the onset of the capacitance increase that would correspond to the onset of hole accumulation. The extracted values are listed in Table 1 and plotted as a function of the gate work function *SI Text*. The values span over 0.7 V when passing from gold to calcium. The threshold voltage is extracted from the C-V curves by estimating the charges $Q(V)$ transported through the P3HT layer in the accumulation regime ($V < V_{FB}$) from Eq. **2**:

$$Q(V) = -\int_{-V_{FB}}^{V} C(V)dV \qquad [2]$$

$Q(V)$ is converted in a density of charge carriers at the semiconductor-electrolyte interface and plotted versus voltage (Fig. 1*D*). If we assume that the mobility is little dependent on the gate voltage, then the drain current in a transistor is proportional to the density of charge carriers. Fig. 1*D* displays clear subthreshold regimes in which traps limit the current and an above-threshold regime where all traps are filled leading to an increased current. The threshold voltage is estimated by extrapolating the above-threshold straight line to zero current. The corresponding data are given in Table 1 and plotted versus the flat-band potential in Fig. 2*E* and as a function of the gate work function *SI Text*. Note that the slope of the line should be proportional to the charge carrier mobility. Parallel lines indicating equal mobility are indeed observed with Au, Ti, and Cu. The decrease of the slope with Ni, Al, and Ca is an artifact coming from the fact that the capacitance is limited by the metal-electrolyte interface.

Influence of the Gate Metal on Electrolyte-Gated OFETS. Our electrolyte-gated OFETs are manufactured in a bottom-contact, top-gate configuration. Interdigitated electrodes are used here (Fig. 2*A*), and the channel length and width are 2 μm and 15 mm, respectively. The gate area is 0.42 mm^2, which is much higher than that of the transistor channel (0.03 mm^2) so that the resulting capacitance is always that of the double-layer at the P3HT side whichever the nature of the metal at the gate. The transfer characteristic is presented for OFETs with Au and Ca-gate electrodes (Fig. 2*B*). Both transistors show typical p-channel behavior. The transistor with an Au-gate switches on at a positive V_{GS}, whereas the transistor including a Ca gate turns on at a relatively more negative V_{GS}. These results are in line with the corresponding flat-band potentials. As a result, the drain current of the transistor with an Au-gate is 500 times higher than that of the device with a Ca-gate at $V_{GS} = 0$ V. The output curves are presented for both transistors (Au, Fig. 2*C*, Ca, and Fig. 2*D*). The superlinear shape of the output curves at high V_{GS} and low V_{DS} is attributed to contact resistance. The threshold voltage V_{TH} can be extracted from the transfer curve plotted in the linear scale (*SI Text*). It is important to extract it from the linear regime, where the charge distribution is uniform along the channel and not from the saturation regime where a nonuniform charge density within the channel may lead to an erroneous extraction. The extrapolation in the linear regime (ELR) method is used to extract the threshold voltage, and the resulting threshold voltage is plotted as a function of the flat-band potential for all six metals (*solid black line*, Fig. 2*E*) and as a function of the gate work function *SI Text*. Five transistors were characterized for each metal in order to obtain statistical data. A clear linear dependence is found with a slope close to unity between the threshold voltage and the flat-band potential.

The deviation of the V_{TH} from the V_{FB} is tentatively attributed to the presence of charge traps. We find two tentative explanations for the difference between V_{TH} determined from the capacitance ($V_{TH\,capa}$) and the transfer curve of the transistor ($V_{TH\,tran}$). One might come from an erroneous extraction of $V_{TH\,tran}$ due to the method used. Indeed, the ELR method is sensitive to gate leakage in short-channel devices and might lead to an overestimation of V_{TH}. On the other hand, in the case of Ni, Al, and Ca, the resulting capacitance in the accumulation regime is that of the (oxidized) metal instead of that of the double-layer at the P3HT electrode could lead to an inaccurate estimation of $V_{TH\,capa}$. For the devices presented, the V_{TH} variation extends over almost 1 V, which corresponds to half of the entire operating voltage regime.

Table 1. Data extracted from C-V and transistor measurements for the various metals

Metal	V_{FB} (V)	$V_{TH\,capa}$ (V)	$V_{TH\,tran}$ (V)
Au	0.73	0.41	0.40 ± 0.08
Ni	0.65	0.42	0.31 ± 0.10
Cu	0.52	0.15	0.28 ± 0.14
Ti	0.31	0.09	−0.14 ± 0.10
Al	0.26	0.10	−0.19 ± 0.15
Ca	0.08	−0.15	−0.53 ± 0.07

The error in $V_{TH\,tran}$ is the standard deviation obtained from five transistors

Unipolar Inverters Based on Electrolyte-Gated OFETs. The ability to tune the V_{TH} of an OFET is of great interest when designing integrated circuits. Complementary circuit design, which includes n- and p-channel transistors, dominates the electronic industry today; however, unipolar circuits are generally easier to manufacture and are sufficient for analyzing the impact of the modification of the V_{TH}. Hence, in this work, logic inverters, in many respects the simplest kinds of integrated circuits, that use a unipolar circuit design are analyzed. An inverter has two components: a load (L) and a driver (D). The driver is a transistor, typically of enhancement mode type, whereas the load can be a resistor or another transistor. Two load transistor configurations are possible: the diode-load and the depleted-load (or zero-gate load). The latter configuration shows better static behavior but is typically slower to switch (28), and is used in this work. In the depleted-load configuration (Fig. 3*A inset*), the gate of the load transistor is connected to its own source; thus, $V_{GS} = 0$ V at all times. As long as $V_{OUT} > V_{DD} + V_{TH,L}$, V_{OUT} (being the output voltage), V_{DD} (the supply voltage), and $V_{TH,L}$ the threshold voltage of the load transistor, the current through the load increases linearly with the voltage. When $V_{OUT} < V_{DD} + V_{TH,L}$ the current saturates. The load and driver transistors can simply be seen as two resistors connected in series. The basic working mechanism of the inverter is input control over voltage division. Thus, adjusting the resistance of the driver transistor via the input

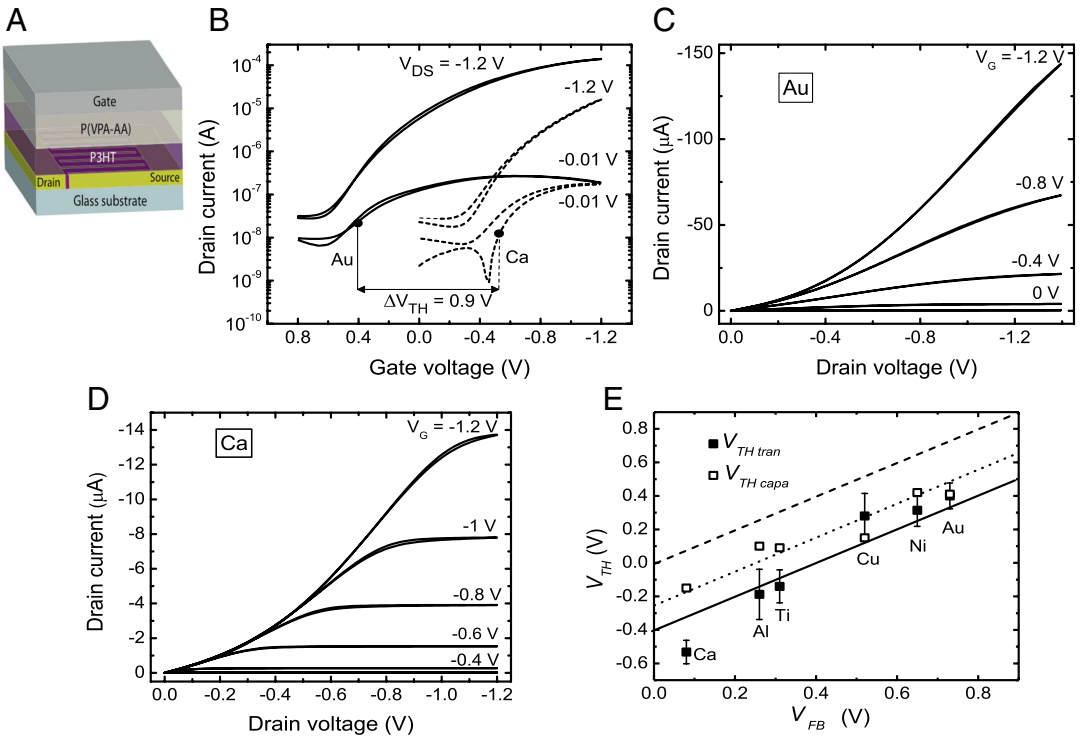

Fig. 2. Electrolyte-gated OFETs with various metals. (*A*) Schematic representation of the OFET. (*B*) Transfer characteristics, in the linear regime ($V_{DS} = -0.01$ V) and at saturation ($V_{DS} = -1.2$ V) for electrolyte-gated OFETs with Au (full line) and Ca (dashed line) as gate metal. Output characteristics for electrolyte-gated OFET with (*C*) Au and (*D*) Ca as gate metal. (*E*) Variation of the threshold voltage extracted from the capacitance, $V_{TH\ capa}$, (empty squares) and transistor measurements, $V_{TH\ tran}$, (full black squares) as a function of the flat-band potential. The dotted and full lines are linear fits with a slope of 1 to the data corresponding to capacitance and transistor measurements, respectively. The dashed line represents the ideal case where $V_{TH} = V_{FB}$.

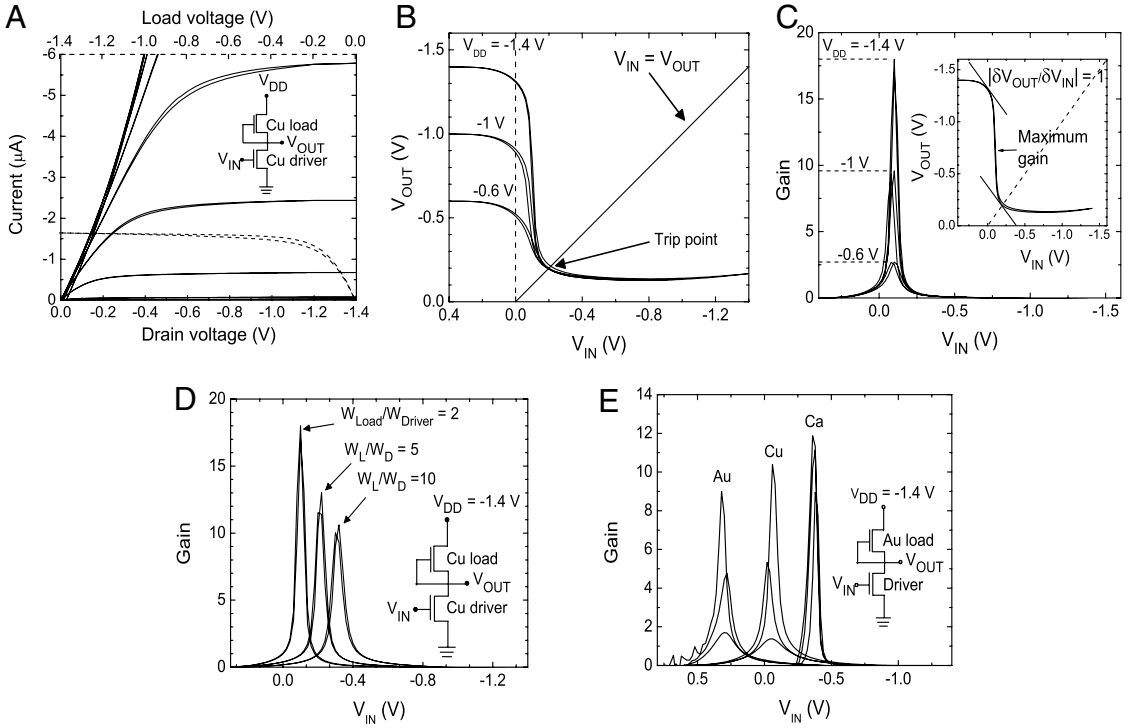

Fig. 3. Inverters based on electrolyte-gated OFETs with various metals. Characteristics of inverters having Cu as the gate electrode metal. (*A*) Output curves (full lines) for the driver transistor together with the load line (dashed line) of the load transistor. The *inset* shows a schematic representation of the inverter circuit. (*B*) Voltage-transfer characteristics and (*C*) signal gain of the inverter for supply voltages ranging from −0.6 to −1.4 V. The *inset* in (*C*) indicates the key parameters of an inverter. (*D*) Influence of a change in the load to driver channel width ratio (from 2 to 10). (*E*) Modification of the signal gain of an inverter with Au as the gate metal for the load and Au, Cu, or Ca as the gate metal for the driver.

voltage essentially controls the inverter output voltage. For example, for an input voltage close to 0 V, the driver and the load have $V_{GS} = 0$ V. Because the load is a depletion-like transistor that is already on at 0 V, the channel resistance of the driver transistor is high and larger than that of the load transistor. Consequently, the voltage drop will mainly occur over the driver giving an output voltage close to the supply voltage (V_{DD}). For an input voltage close to V_{DD}, the driver is strongly switched on and its channel resistance is low and smaller than that of the load that sets the output node close to 0 V. Ideally, the voltage swing, i.e., the voltage difference between the high and low output levels, should be equal to the supply voltage. The current through the load (*dashed line*) and through the driver (*solid lines*) of an inverter based on transistors with copper gate electrodes are presented in Fig. 3*A*. Because, in an inverter, the current through the load and the driver should be the same, the intersection of the two curves determines the value of V_{OUT} for a given V_{IN}. The voltage-transfer characteristic (VTC) of the inverter, i.e., the output voltage (V_{OUT}) as a function of the input voltage (V_{IN}), is displayed in Fig. 3*B*. The VTC gives information about the static performance of the inverter. In our case, the high output level is close to V_{DD}, but the low output level at high V_{IN} is noticeably larger than 0 V. This is likely an effect of the superlinear output curves caused by a high contact resistance of the driver transistor. Another key parameter for inverters is the signal gain, which is defined as $A = |\delta V_{OUT}/\delta V_{IN}|$ (Fig. 3*C inset*). Inverters that show a gain larger than unity can be used for driving other gates in logic circuits. The switching threshold, which is the voltage at which the inverter switches from low to high output and displays maximum gain, should ideally coincide with the trip point and be positioned at half of the supply voltage in order to provide optimum noise margins. For the inverter in Fig. 3*B*, the transition occurs for an input voltage of only about −0.1 V that is due to the positive threshold voltage of the driver transistor, leads to poor noise margins. Various methods have been investigated to remedy this issue. The most common one is to increase the resistance of the driver transistor by reducing its channel width (relative to that of the load transistor). Typically, a ratio of 10 is chosen between the load and the driver channel width. The gain for inverters with various channel width ratios is shown Fig. 3*D*. When increasing this ratio from two to 10, the switching threshold is shifted from −0.1 V to −0.3 V, which provides better noise margins. A downside of this approach is that one transistor becomes much larger than the other, which limits miniaturization of the system. The use of a level-shifter is another widespread method that requires two additional transistors and an additional power supply (29). Other methods aim at adjusting the V_{TH} of the driver and load transistors. The driver transistor should have a negative threshold voltage in order for its resistance to be high at low-input voltages; however, the load transistor should operate in a depletion-like mode to make its resistance low. Therefore, a positive V_{TH} of the load transistor is beneficial. This can be achieved by changing the dielectric surface of one of the transistor (30) using a dual gate transistor (31) performing photo-treatment (32) or by taking use of different thicknesses of the semiconducting layer (33).

Another way to accomplish control over V_{TH} is to exploit the difference in V_{TH} by using different gate electrode metals in the driver and in load transistors (26). We built inverters in which Au always was used as the gate material for the load transistor. Here, the resulting positive threshold voltage induces a low channel resistance of the load transistor. Au, Cu, or Ca was used as the gate electrode metal in the driver transistor in order to provide a variety of threshold voltages ranging from positive to negative values. Note that the driver and the load transistors have the same channel geometry ($W = 15$ mm and $L = 2$ μm). The gain, as a function of the input voltage for each inverter, is given in Fig. 3*E* for a supply voltage of $V_{DD} = -1.4$ V. The inverter with an Au-gate electrode on the driver and load transistors shows a positive switching threshold voltage that makes it unsuitable for use in logic circuits. Using a driver transistor with a copper gate electrode that has a positive V_{TH} but that is smaller than that for an Au-gate shifts the switching threshold towards more negative voltages allowing it to be used in logic circuits; however, the ideal $V_{DD}/2$ (i.e. −0.7 V) value is far from being reached. The use of a driver transistor with a negative V_{TH} such as the one with a Ca gate should diminish this problem. The OFET with a Ca-gate electrode exhibit a much more negative V_{TH} ($V_{TH} = -0.53$ V) resulting in a high-channel resistance at low-input voltages. By changing from an Au to a Ca-gate electrode in the driver transistor leads to a shift of the inverter switching (gain maximum) from +0.3 V to −0.36 V. For this W-L configuration, it should be possible to shift the gain maximum further towards $V_{DD}/2$ (−0.7 V) by using a metal with a work function even higher than that of Au, for instance using Pt as the gate electrode material in the load transistor. Off course, another strategy is to choose a metal electrode with a lower work function than that of Ca for the gate of the driver transistor. Moreover, a semiconductor with a relatively higher ionization potential should shift the voltages to more negative values.

Conclusions

In summary, systematic control of the threshold voltage in polyelectrolyte-gated OFETs has been demonstrated by changing the work function of the gate electrode. It is possible to shift the threshold voltage by as much as 0.9 V when changing from Au to Ca. This equals half of the entire operation voltage range of the electrolyte-gated OFETs studied. Tuning the threshold is of general interest in designing analogue and digital circuits. In particular, threshold voltage tuning is of importance in the case of zero-load inverters where positive and negative threshold voltages are advantageous for the load and driver transistors, respectively. This implies that the dimensional ratio of the load and the driver transistor channels is no longer of significant importance, which then enables size reduction of circuits.

Materials and Methods

Materials. Regioregular P3HT (electronic grade, 99.995% trace metal basis) was purchased from Sigma-Aldrich, dissolved in 1,2-dichlorobenzene (10 mg·ml^{-1}), and filtered with a 0.2 μm polytetrafluoroethylene syringe filter. P(VPA-AA) was purchased from Rhodia, dissolved in a mixture of water and 1-propanol (40 mg·ml^{-1}) with a solvent ratio of 1:4, and filtered with a 0.2 μm nylon syringe filter

Device Manufacturing. 5 nm thick titanium (attachment layer) and 50 nm thick gold films were formed on borosilicate glass substrates (DESAG D263). Contacts are defined by photolithography and wet etching. For the capacitor structure, the effective surface is 0.0004 cm^2. For the transistor structure, interdigitated source and drain electrodes are used, with a channel length and width of 2–3 μm and 15 mm, respectively. The P3HT solution is heated to 60 °C and spin coated on the photolithography-patterned substrates (substrates were heated to 150 °C prior to spin coating) at 2000 rpm for 30 s resulting in a film thickness of 30 nm. The film was then dried at 120 °C under nitrogen for 20 min to get rid of the residual solvent. A 135 nm thick film of P(VPAAA) was obtained by using a speed of 2000 rpm for 1 min. The film was then dried under vacuum at 120 °C for 120 s. An 80 nm thick top electrode for the capacitors and gate electrode for the transistors are formed by thermal evaporation of various metals through a Ni shadow mask (Tecan Ltd.). Interconnects between the gate, source and drain electrodes were formed by thermal evaporation of titanium through a second shadow mask.

Measurements. The electrical characteristics of the transistors and the inverters were measured using a semiconductor parameter analyzer (Keithley 4200-SCS). The impedance measurements were carried out with an Alpha high-resolution dielectric analyzer (Novocontrol GmbH). An AC voltage of 0.001 V was applied, the frequency was set at 1 kHz, and the DC voltage was swept from positive to negative voltages. An equivalent circuit model made of a resistor and a capacitor in parallel was used to extract the effective capacitance, which was calculated from the equation $C = 1/(2\pi f Im(Z))$ and where f is the frequency and Z is the measured impedance.

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