Supporting Information

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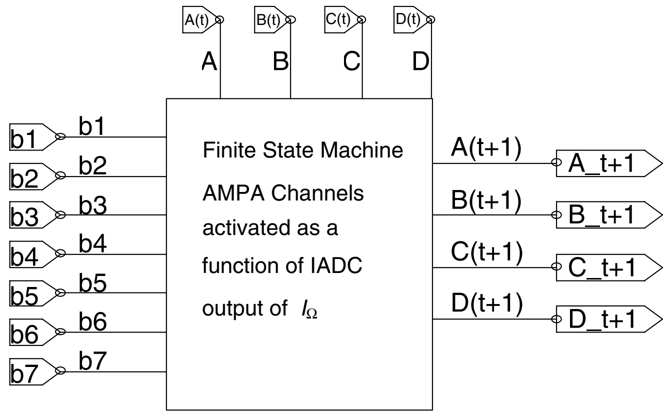

Fig. S1. A finite state machine (FSM) is a digital circuit that takes the current state of the world, in this case the activation levels of the AMPA channels A(t), B(t), C(t), and D(t), and adds new inputs (e.g., the digitized I_Ω output from the IADC, marked as b1 ..... b7), to form the next state of the AMPA channels ($A(t+1)$, $B(t+1)$, $C(t+1)$, $D(t+1)$). In our model, the opening or closing of individual AMPA channels are controlled by the inputs according to the code shown in Table S1. For example, the highlighted inputs in Table S1 will result in a new state of the AMPA channels as shown in Table S1.

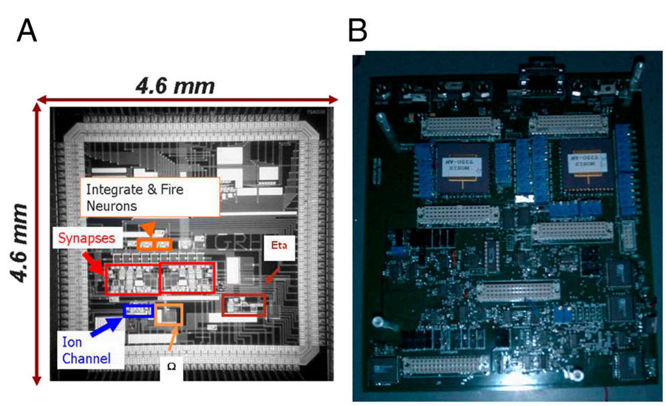

Fig. S2. (*A*) Picture of fabricated chip, including AMPA, NMDA, calcium, omega, eta, and somatic circuits and test circuits. (*B*) Circuit board for testing the chip.

Table S1. Truth table for the FSM in Fig. S1 showing potentiation/depression of the AMPA channels based on the inputs b1–b7

B1	B2	B3	B4	B5	B6	B7	dW
0	0	0	0	0	0	0	depress by 4
0	0	0	0	0	0	1	depress by 3
0	**0**	**0**	**0**	**0**	**1**	**1**	**depress by 2**
0	0	0	0	1	1	1	depress by 1
0	0	0	1	1	1	1	stay the same
0	0	1	1	1	1	1	potentiate by 1
0	1	1	1	1	1	1	potentiate by 2
1	1	1	1	1	1	1	potentiate by 3

Table S2. Update of A(t), B(t), C(t), and D(t) to yield A($t+1$), B($t+1$), C($t+1$), and D($t+1$), given inputs b1–b7 as highligted in Table S1

A(t)	B(t)	C(t)	D(t)	b1	b2	b3	b4	b5	b6	b7	A(t+1)	B(t+1)	C(t+1)	D(t+1)
1	1	1	1	*0*	*0*	*0*	*0*	*0*	*1*	*1*	**0**	**0**	**1**	**1**